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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,627	12/16/2003	Etsuko Asano	740756-2688	2662

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EXAMINER	
PERKINS, PAMELA E	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 08/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/735,627	ASANO ET AL.	
	Examiner	Art Unit	
	Pamela E. Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) *26-36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/25/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the amendment on 25 April 2006. Claims 1-36 are pending; claims 26-36 are withdrawn from consideration.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 16 and 21 rejected under 35 U.S.C. 103(a) as being obvious over Nakamura et al. (6,887,724) in view of Yamazaki et al. (2003/0207502).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer

in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Nakamura et al. disclose an evaluation method of a TFT characterized by a step of forming a TEG (351) and the TFT (251) over a same substrate (201/301), each having a gate electrode (219/324) over a semiconductor film (205/304) which is formed to have a low concentration impurity region (col. 4, line 65 thru col. 5, line 14), a step of measuring resistance of the low concentration impurity region of the TEG, and estimating an impurity concentration of the low concentration impurity region of the TFT by the resistance (FIG. 7A-10D; col. 18, lines 23-54). Nakamura et al. does not disclose a low concentration impurity region overlapping the gate electrode.

Yamazaki et al. disclose a method of manufacturing a TFT characterized forming a TFT over a substrate, having a gate electrode (204) and has a low concentration impurity region overlapping the gate electrode (("GOLD") gate-drain overlapped LDD) (para. 7-10).

Since Nakamura et al. and Yamazaki et al. are both from the same field of endeavor, a method of manufacturing a TFT, the purpose disclosed by Yamazaki et al. would have been recognized in the pertinent art of Nakamura et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nakamura et al. by forming a low concentration impurity region overlapping the gate electrode of the TFT as taught by Yamazaki et al. to improve the reliability of the TFT and increase the hot carrier tolerance (para. 9 &10).

Referring to claim 16, Nakamura et al. disclose the TEG has a test element for measuring resistance of a low concentration impurity region (col. 18, lines 23-54).

Referring to claim 21, Nakamura et al. disclose a method of manufacturing a semiconductor device characterized by having a TFT manufactured by using the evaluation method (col. 2, lines 19-65).

Claims 2-6, 11-14, 17-19 and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. in view of Yamazaki et al., further in view of Nishimura et al. (6,462,802).

Nakamura et al. in view of Yamazaki et al. disclose the subject matter claimed above except each having a gate electrode that is laminated with a first conductive film and a second conductive film each having a taper over a semiconductor film, wherein an edge of the first conductive film extends over an edge of the second conductive film.

Referring to claims 2, 4 and 5, Nishimura et al. disclose a method of forming a TFT where a TFT (101) is formed over a substrate (103), having a gate electrode that is laminated with a first conductive film (107) and a second conductive film (108) over a semiconductor film (105) overlapping the gate electrode, wherein an edge of the first conductive film (107) extends over an edge of the second conductive film (108), wherein a side edge portion of the semiconductor film is provided between the edge of the first conductive film and the edge of the second conductive film (FIG. 1; col. 12, line 65 thru col. 13, line 13).

Since Nakamura et al. and Nishimura et al. are both from the same field of endeavor, a method of forming a TFT, the purpose disclosed by Nishimura et al. would have been recognized in the pertinent art of Nakamura et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nakamura et al. by a gate electrode that is laminated with a first conductive film and a second conductive film each having a taper over a semiconductor film, wherein an edge of the first conductive film extends over an edge of the second conductive film as taught by Nishimura et al. to prevent thermal oxidation (col. 1, line 64 thru col. 2, line 20).

Referring to claims 3 and 6, Nakamura et al. disclose the first conductive film is formed from a TaN film and the second conductive film is formed from a W film (col. 12, lines 32-44).

Referring to claims 11-14, Nishimura et al. disclose a correlation of the resistance and an overlapping position of the first conductive film or the second conductive film and the semiconductor film is obtained (col. 6, lines 23-27; col. 11, lines 45-59).

Referring to claims 17-19, Nakamura et al. disclose the TEG has a test element for measuring resistance of a low concentration impurity region (col. 18, lines 23-54).

Referring to claims 22-24, Nakamura et al. disclose a method of manufacturing a semiconductor device characterized by having a TFT manufactured by using the evaluation method (col. 2, lines 19-65).

Claims 7-10, 15, 20 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. in view of Yamazaki et al. further in view of Nishimura et al. and Fujikawa et al. (6,836,140).

Nakamura et al. in view of Yamazaki et al. and Nishimura et al. disclose the subject matter claimed above except a plurality of first to third TEGS is provided.

Referring to claims 7 and 8, Fujikawa et al. disclose an evaluation method of a TFT characterized by a step of forming a TEG and the TFT over a same substrate, each having a gate electrode; a step of measuring resistance of the low concentration impurity of the first TEG; a step of measuring resistance of the channel forming region of the second TEG; a step of measuring resistance of the impurity region of the third TEG (col. 10, lines 25-41; Table 1).

Since Nakamura et al. and Fujikawa et al. are both from the same field of endeavor, an evaluation method of a TFT, the purpose disclosed by Fujikawa et al. would have been recognized in the pertinent art of Nakamura et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nakamura et al. by a plurality of first to third TEGS is provided as taught by Fujikawa et al. to increase TFT production efficiency (col. 2, lines13-22).

Referring to claim 9, Nakamura et al. disclose the first conductive film is formed from a TaN film and the second conductive film is formed from a W film (col. 12, lines 32-44).

Referring to claim 10, Nishimura et al. disclose edges of a first conductive film and a second conductive film having a taper (FIG. 1; col. 12, line 65 thru col. 13, line 13).

Referring to claims15, Nishimura et al. disclose a correlation of the resistance and an overlapping position of the first conductive film or the second conductive film and the semiconductor film is obtained (col. 6, lines 23-27; col. 11, lines 45-59).

Referring to claim 20, Nakamura et al. disclose the TEG has a test element for measuring resistance of a low concentration impurity region (col. 18, lines 23-54).

Referring to claim 25, Nakamura et al. disclose a method of manufacturing a semiconductor device characterized by having a TFT manufactured by using the evaluation method (col. 2, lines 19-65).

Response to Arguments

Applicant's arguments, see the paper filed 25 April 2006, with respect to the rejection(s) of claim(s) 1-25 under 35 U.S.C. 102(e) and 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Yamazaki et al. (2003/0207502).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571)

272-1840. The examiner can normally be reached on Monday thru Friday, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Soniae M. Thomas
Art Unit 2822

PEP
14 August 2006